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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/665,654
Filing Date: September 18, 2003
Appellant(s): CHEN ET AL.

Jon A. Gibbons
For Appellant

EXAMINER'S ANSWER

This is in response to the supplemental appeal brief filed 9/10/2007 appealing from the Office action mailed 10/17/2005.

The arguments in the supplemental appeal brief did not change from the original appeal brief, filed 5/3/2006, therefore the arguments in this examiner answer are identical to the arguments set form in the original examiner answer, sent 7/7/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of claims contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 4,431,973	Goto et. al.	02-1984
US 5,602,798	Sato et al.	02-1997
US 5,724,108	Shibata	03-1998
US 5,952,854	Kubota et al.	09-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

This is a reply to Applicant's amendment filed on 09/08/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in tiffs country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798).

With respect to claim 1, 9 and 10, Sato et al. discloses, in Fig. 14A and col. 14, fines 35-36, a circuit arrangement comprising a) an input signal [ID1] to be delayed and b) a series of at least two delay stage [60a-60n], wherein each of the delay stages includes a stack of uniform

("same structure "; see col. 14, lines 35-36) transistors [P3, N1] with a first group of a first conductivity type [p-channel] and a second group of transistors of a second conductivity type [n-channel] without using extended channel length transistors in the .delay stages so that, as a result, tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors, as a result, provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip; wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages, wherein a source of a top transistor in the stack is coupled to a first reference voltage [Vcc], wherein a source of a bottom transistor in the stack is coupled to a second reference voltage [ground], and wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage; wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claim 2, Sato et al. discloses, in Fig. 14A, that each stack of transistors includes additional transistors electrically coupled with the top transistor [P3] and the bottom transistor IN1]; wherein a drain of a first additional transistor [P2] is electrically coupled to a source of the top transistor, a drain of the last additional transistor IN2] is connected to a source of the bottom transistor, and wherein a drain of each of zero or more remaining additional

transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack.

With respect to claims 3-6, Sato et al. discloses, in Fig. 14A, that delay elements comprised both n-channel FET and p-channel FET.

With respect to claims 7 and 8, Sato et al. discloses, in Fig. 14A, that the input signal to 'be delayed is a clock signal.

With respect to claim 11, Sato et al. discloses, in Fig. 14A and col. 14, lines 35-36, a delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising a first transistor [P3] with a source electrically coupled to a first reference voltage [Vcc]; a last transistor [N 1] with a source electrically coupled to a second reference voltage [Ground]; a totem pole of at least two transistors, the totem pole including: a top transistor [P2] with a source electrically coupled to a drain of the first transistor; a bottom transistor [N2] with a source electrically coupled to a drain of the last transistor and at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a uniform *("same structure "; see col. 14, lines 35-36)* channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that, *as a result,* tolerances across the delay stages track tolerate of other delay circuits on a chip, the use of uniform channel length transistors, *as a result,* provides uniform tolerance variations and increase parametric tracking of device characteristics including delays in timing circuits across

the other delay circuits; an input electrically coupled to each gate within the totem pole; and an Output electrically coupled to connection between one source and one drain of two transistors within the totem pole; wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive: and wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claims 12-14, Sato et al. discloses, in Fig. 14A, that delay elements comprised both n-channel FET and p-channel FET.

(10) Response to Arguments

With respect to claim 1, on page 5, the Appellants assert that Sato does not teach, suggest, or anticipate the claimed limitations, particularly the claim limitations of:

"wherein each of the delay stages includes a stack of uniform channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip".

The Examiner disagrees. As clearly shown in Fig. 14A of Sato et al., each of the delay stages includes a stack of uniform *(".same structure ", see col. 14, lines 35-36; "same size ", see col. 14, lines 65-66)* transistors [P3, N1] With a first group of a first conductivity type [p-

channel] and a second group of transistors of a second conductivity type [n-channel] without using extended channel length transistors in the delay stages so that, *as a result,* tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors, *as a result,* provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip.

Still with respect to claim 1, at the end of second paragraph on page 5, the Appellants state that *"Sato is silent on "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip*" and "*The Appellants respectfully contend that "the same structure" as taught by Sato is not the same as "uniform channel length transistors"*. The Examiner respectfully disagrees. Sato's Fig. 14A discloses a delay element, in which the delay stages [60a - 60n] have the same structure (col. 14, lines 35-36) and the transistors of the delay stages have the same size (col. 14, lines 65-66); "same size" connotes same channel length and same channel width *(i.e. a) Goto et al. (US Pat. No. 4,431,973), col. 5, lines 14-15; b) Shibata (US Pat. No. 5,724,108), col. 11, lines 51-52; and c) Kubota et al. (US Pat. No. 5,952,854), col. 13, lines 43-44);* therefore, the Examiner contends that the language is expressly stating that Sato's each delay stage [60a - 60n] includes a stack of uniform channel length transistors. Furthermore, since Sato discloses the delay element of the claimed invention with the use of uniform channel length transistors; thus, Sato discloses the delay element with the use of uniform channel length transistors, which provides uniform

tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip.

Similar point of traversal referencing "*Sato never mentions the channel length of a transistor and is completely silent on "each of the delay stages includes a stack of uniform channel length transistors*" has been addressed regarding claim 1, on page 9, first paragraph. It is suggested to refer to the Examiner's response stated in the above paragraph.

Still with respect to claim 1, the Appellants state, in the first paragraph of page 9, that "There is no teaching that the "channel length" of the gate circuits are identical to channel length of other transistors **outside** the delay element". It is noted that the features upon which Appellants relies (i.e., other transistors outside the delay element) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Still with respect to claim 1, the Appellants state, in the second paragraph of page 9, that "Sato is completely silent on "without using extended channel length transistors in the delay stages" and "Sato never explicitly states or implies that extended channel length transistors are not used.". Sato is completely silent on using extended channel length transistors; therefore, it is evident that his delay circuit is configured without using extended channel length transistor.

Similar point of traversal referencing *" nowhere does Sato teach uniform channel length transistors are used "* has been addressed regarding claim 1, on page 9, second paragraph. It is suggested to refer to the Examiner's response stated in the above paragraph.

Again, similar point of traversal referencing *"Sato does not teach or suggest "the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip"* has been addressed regarding claim 1, on page 10, second paragraph.

It is suggested to refer to the Examiner's response stated in the above paragraph.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

The reference to Sato et al. discloses a delay element that meets all limitations of the appealed claims.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ryan C. Jager/

Conferees:

Drew Richards

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER

David Blum

Ryan C. Jager RCJ